

AT/ 2813

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Guoqiang Xing, et al.

Docket No: TI-31729

Serial No: 09/901,416

Conf. No: 7364

Examiner: Thanh T. Nguyen

Art Unit: 2813

Filed: 07/09/2001

For: DUAL HARDMASK PROCESS FOR THE FORMATION OF COPPER/LOW-K  
INTERCONNECTS

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**REPLY BRIEF**

Mail Stop Appeal Brief - Patents  
Commissioner For Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)**

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 1-20-04.

  
Ann Trent

Dear Sir:

The following Reply Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the Examiner's Answer mailed December 3, 2003.

**REMARKS**

In forming the rejections to the claims on appeal the examiner argued that the Flanner et al. patent taught in Figures 3-12, a method of forming interconnects that comprises the use of antireflective layers 4 and 6 as hardmask layers to etch a trench (20). The appellants in the appeal brief argued that as described in Figures 3-12, the antireflective coating layers 4 and 6 are not acting as masking layers as these layers are masked by the photoresist layer 2 during the entire etching process. In the examiner's reply the examiner no longer argues this point and apparently concurs with

the appellants on this point. In responding to the appellants brief, the examiner now argues that it is the process in Figures 20 and 21 of the Flanner et al. patent that shows the use of the antireflective layers 4 and 6 as hardmask layers. The examiner then compares the process illustrated in Figures 20 and 21 of the Flanner et al. patent with the process illustrated in Figures 1(a) to 1(c) of the application under appeal.

As understood by persons of ordinary skill in the semiconductor arts, a mask is used to transfer a pattern to an underlying layer. This is illustrated in Figures 3-6 of the Flanner et al. patent where the masking photoresist layer 2 is used to transfer the pattern to the underlying layers through the etch process. In Figures 9-13 of the Flanner et al. patent, masking layer 30 is used to transfer the pattern to the underlying layers through an etch process (described in col. 6, lines 39-59 of the Flanner et al. patent). This is further illustrated in the application on appeal in Figure 1(d) where the masking layer 60 is used to transfer the pattern to the underlying layer 40, and in Figure 1(c) where the masking layer 85 is used to transfer the pattern to the underlying layers.

In referring to Figures 20 and 21 in the Flanner et al. patent, the examiner argues that "[F]lanner further teaches in figures 20 and 21 that after removing the photoresist layer 2, he uses only first and second hardmask patterned layers 4 and 6 as masks to remove the remaining portion (A) of the dielectric layer 12 and dielectric layer 14 to form the trench/via." The examiner is incorrect in describing the process shown in Figures 20 and 21. Referring to Figure 17 in the Flanner et al. patent, the photoresist layer 2 is used as a masking layer to transfer the pattern to the underlying layers. In Figure 18, an addition photoresist layer 300 is formed and used as a masking layer to transfer the pattern into the underlying layer 12 through an etch process. Following the removal of the masking layer 300, the remaining portion of (A) of the dielectric layer is removed using an unmasked blanket dielectric etching step. Clearly layers 4 and 6 are not acting as masking layers as it was the photoresist masking layer 300 that was used as a masking layer during the transfer of the via pattern during the formation of the via. The examiner is therefore incorrect in the assertion that layers 4 and 6 are acting as masking layers in Figures 20 and 21 of the Flanner et al. patent. Further the examiner

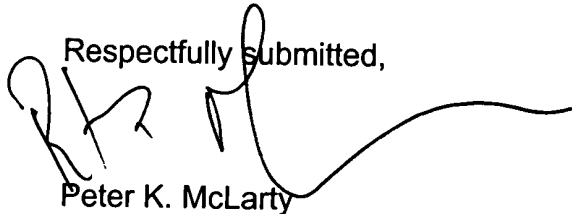
has concurred with the appellants with regards to the purpose of the masking layer as illustrated in Figures 3-12 of the Flanner et al. patent. As such the appealed claims are allowable over the cited art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the application is now in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Peter K. McLarty', with a long horizontal flourish extending to the right.

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